CLAIMS:

What is claimed is:

1. A method of making a device comprising:
providing a substrate;
forming nanoclusters over the substrate;
depositing an oxidation barrier layer over the nanoclusters;
patterning to form a first area and a second area, the first area including the oxidation barrier layer and the nanoclusters over the substrate, and the second area having the oxidation barrier layer and the nanoclusters removed;
forming a second dielectric over the first area subsequent to the patterning; and
removing at least a portion of the oxidation barrier layer from the first area subsequent to the forming the second dielectric, wherein the removing the at least a portion at least reduces a thickness of the oxidation barrier layer.

2. The method of claim 1, wherein the nanoclusters include at least one selected from a group consisting of silicon nanocrystals, germanium nanocrystals, silicon and germanium alloy nanocrystals, and metal nanocrystals.

3. The method of claim 1 wherein the forming the second dielectric includes subjecting the oxidation barrier layer to a temperature of 600°C or greater.

4. The method of claim 1, wherein the oxidation barrier layer includes at least one selected from a group consisting of silicon nitride, silicon oxynitride, silicon, a silicon germanium alloy, a high-K dielectric material, and a metal.

5. The method of claim 4, wherein the high-K dielectric material includes at least one selected from a group consisting of hafnium oxide, lanthanum oxide, lanthanum aluminate, tantalum pentoxide, zirconium silicate, lanthanum silicate, aluminum oxide, zirconium oxide, zirconium silicate, tantalum oxide, and titanium oxide.

6. The method of claim 4, wherein the metal includes at least one selected from a group consisting of tantalum, tungsten silicide, molybdenum silicide, nickel, nickel silicide, cobalt, cobalt silicide, iridium, iridium oxide, ruthenium, ruthenium oxide, and titanium.

7. The method of claim 1, wherein the oxidation barrier layer has a thickness of 2 nanometers or greater.

8. The method of claim 1, further comprising: forming transistors in the first and second areas.

9. The method of claim 8, wherein transistors in the first area include charge storage transistors, wherein portions of the nanoclusters are utilized as charge storage locations for the charge storage transistors.

10. The method of claim 8, wherein the transistors in the second area includes transistors having a gate dielectric that includes portions of the second dielectric.

11. The method of claim 1, wherein the removing at least a portion of the oxidation barrier layer from the first area includes removing at least substantially all of the oxidation barrier layer from the first area.

12. The method of claim 1, wherein the oxidation barrier layer includes a first layer portion and a second layer portion located above the first layer portion, wherein the removing at least a portion of the oxidation barrier layer from the first area includes removing the second layer portion with the first layer portion remaining.

13. The method claim 12 wherein the oxidation barrier layer is oxidized to form the second layer portion.

14. The method of claim 12 wherein the first layer portion is 5 nanometers or less.

15. The method of claim 12 wherein the removing the second layer portion further includes etching the second layer portion with an etch.

16. The method of claim 12 further comprising:
forming a layer of gate material over the first layer portion subsequent to the removing the second layer portion.

17. A method of making a device comprising:
providing a substrate having a structure of nanoclusters and dielectric over the substrate;
depositing an oxidation barrier layer over the structure;
patterning to form a first area and a second area, the first area including the oxidation barrier layer and the structure over the substrate, and the second area having the oxidation barrier layer and at least the nanoclusters of the structure removed;
forming a second dielectric over the first area subsequent to forming the patterning; and
removing at least a portion of the oxidation barrier layer from the first area subsequent to the forming the second dielectric, wherein the removing the at least a portion at least reduces a thickness of the oxidation barrier layer.

18. The method of claim 17, wherein the nanoclusters of the structure include at least one selected from a group consisting of silicon nanocrystals, germanium nanocrystals, silicon and germanium alloy nanocrystals, and metal nanocrystals.

19. The method of claim 17 wherein the forming the second dielectric includes subjecting the oxidation barrier layer to a temperature of 600°C or greater.

20. The method of claim 17, wherein the structure is formed by a method comprising:
forming a bottom dielectric layer over the substrate;
forming nanoclusters over the bottom dielectric layer; and
forming a control dielectric layer over the nanoclusters.

21. The method of claim 20, wherein the bottom dielectric layer and control dielectric layer each include one selected from a group consisting of silicon dioxide, silicon oxynitride, hafnium oxide, aluminum oxide, lanthanum oxide, and lanthanum silicate.

22. The method of claim 17, wherein the nanoclusters are formed by a method comprising:

implanting nanocluster material within the dielectric and subsequently annealing the structure to induce phase separation to form nanoclusters.

23. The method of claim 17, wherein the structure is formed by a method comprising:

forming a bottom dielectric over the substrate;

depositing at least one layer of nanocluster material over the bottom dielectric;

forming a control dielectric over the at least one nanocluster material layer; and

annealing the at least one layer of nanocluster material to form nanoclusters.

24. The method of claim 17, wherein the device includes a memory and wherein the first area includes a memory array area.

25. The method of claim 17, wherein the oxidation barrier layer includes at least one selected from a group consisting of silicon nitride, silicon oxynitride, silicon, a silicon germanium alloy a high-K dielectric material, and a metal.

26. The method of claim 25, wherein the high-K dielectric material includes at least one selected from a group consisting of hafnium oxide, lanthanum oxide, lanthanum aluminate, tantalum pentoxide, zirconium silicate, lanthanum silicate, aluminum oxide, zirconium oxide, zirconium silicate, tantalum oxide, and titanium oxide

27. The method of claim 25, wherein the metal includes at least one selected from a group consisting of tantalum, tungsten silicide, molybdenum silicide, nickel, nickel silicide, cobalt, cobalt silicide, iridium, iridium oxide, ruthenium, ruthenium oxide, and titanium

28. The method of claim 17, wherein the oxidation barrier layer has a thickness of 2 nanometers or greater.

29. The method of claim 17, further comprising:

forming transistors in the first and second areas.

30. The method of claim 29, wherein transistors in the first area include charge storage transistors, wherein portions of the nanoclusters are utilized as charge storage locations for the charge storage transistors.

31. The method of claim 29, wherein the transistors in the second area includes at transistors having a gate dielectric that includes portions of the second dielectric.

32. The method of claim 31 wherein transistors in the first area include charge storage transistors having a bottom dielectric having a thickness, wherein gate dielectrics of transistors of the second area have a thickness greater than the thickness of the bottom dielectric.

33. The method of claim 17, wherein the removing at least a portion of the oxidation barrier layer from the first area includes removing at least substantially all of the oxidation barrier layer from the first area.

34. The method of claim 17, wherein the oxidation barrier layer includes a first layer portion and a second layer portion located above the first layer portion, wherein the removing at least a portion of the oxidation barrier layer from the first area includes removing the second layer portion with the first layer portion remaining.

35. The method claim 34 wherein the oxidation barrier layer is oxidized to form the second layer portion.

36. The method of claim 34 wherein the first layer portion is 4 nanometers or less.

37. The method of claim 34 wherein the removing the second layer portion further includes etching the second layer portion with an etch.

38. The method of claim 34 further comprising:

forming a layer of gate material over the first layer portion subsequent to the removing the second layer portion.

39. A method of making a semiconductor device comprising:

providing a substrate having a structure of nanoclusters and dielectric overlying the substrate,

depositing an oxidation barrier layer over the structure, wherein the oxidation barrier layer includes at least one selected from a group consisting of silicon nitride, silicon oxynitride, silicon, a silicon germanium alloy, a high-K dielectric material, and a metal;

patterning to form a first area and a second area, the first area including portions of the oxidation barrier layer and the structure, and the second area having portions of the oxidation barrier layer and at least the nanoclusters of the structure removed;

forming a second dielectric in the second area subsequent to the patterning; and

removing at least a portion of the oxidation barrier layer from the first area subsequent to the forming the second dielectric, wherein the removing the at least a portion at least reduces a thickness of the oxidation barrier layer.

40. A method of making a semiconductor memory comprising:

providing a substrate having a structure of nanoclusters and dielectric overlying the substrate;

depositing an oxidation barrier layer over the structure;

patterning to form a first area and a second area, the first area including portions of the oxidation barrier layer and the structure, and the second area having portions of the oxidation barrier layer and at least the nanoclusters of the structure removed;

forming a second dielectric outside the first area subsequent to the patterning;

removing at least a portion of the oxidation barrier layer from the first area subsequent to the forming the second dielectric, wherein the removing the at least a portion at least reduces a thickness of the oxidation barrier layer;

forming a charge storage transistor in the first area, wherein at least a portion of the nanoclusters is utilized as a charge storage location for the charge storage transistor;

forming a second transistor in the second area, wherein a portion of the second dielectric serves at least as a portion of a gate dielectric of the second transistor.

41. The method of claim 40 wherein the oxidation barrier layer includes at least one selected from a group consisting of silicon nitride, silicon oxynitride, silicon, a silicon germanium alloy, a high-K dielectric material, and a metal.